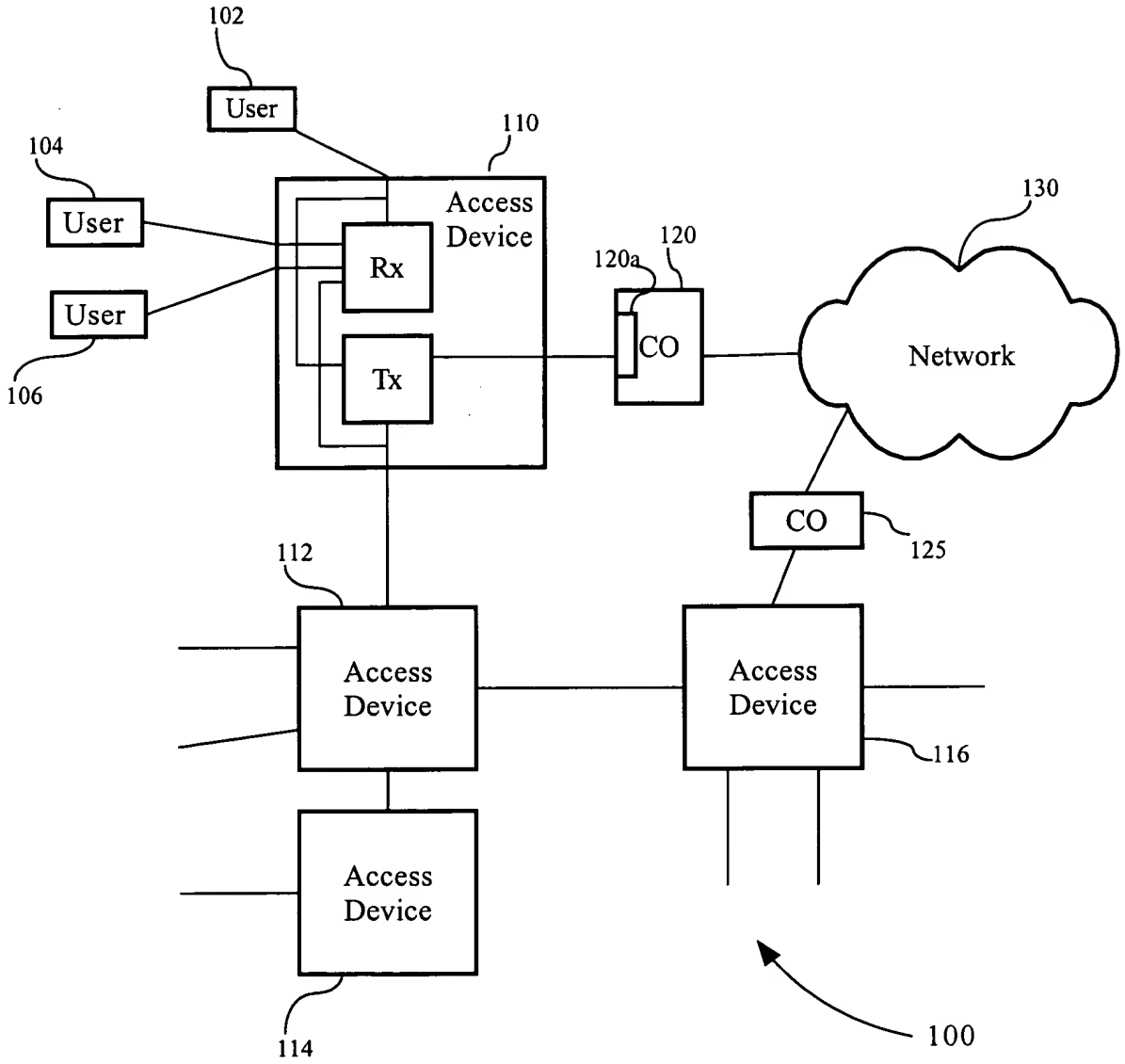
102
User
110
104
Access
Device
User
Rx
130
120
120a
User
CO
Network
106
Tx
CO
125
112
Access
Device
Access
Device
116
Access
Device
114
100

Fig. 1

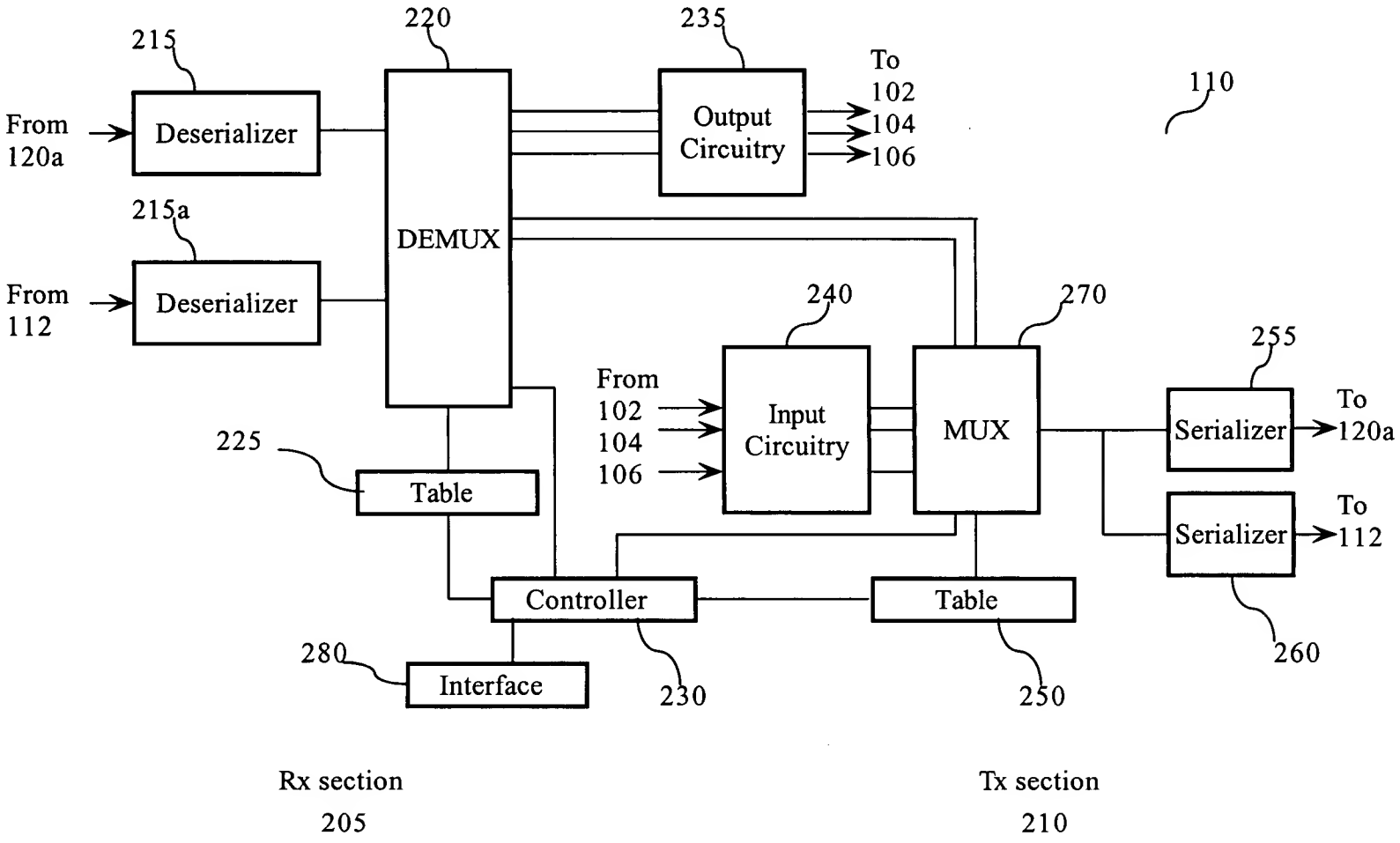
215
220
235
To
102
104
106
110
From
120a
Deserializer
DEMUX
Output
Circuitry
215a
From
112
Deserializer
240
270
255
From
102
104
106
Input
Circuitry
MUX
Serializer
To
120a
225
Table
Serializer
To
112
Controller
Table
280
Interface
230
250
260
Rx section
205
Tx section
210

Fig. 2

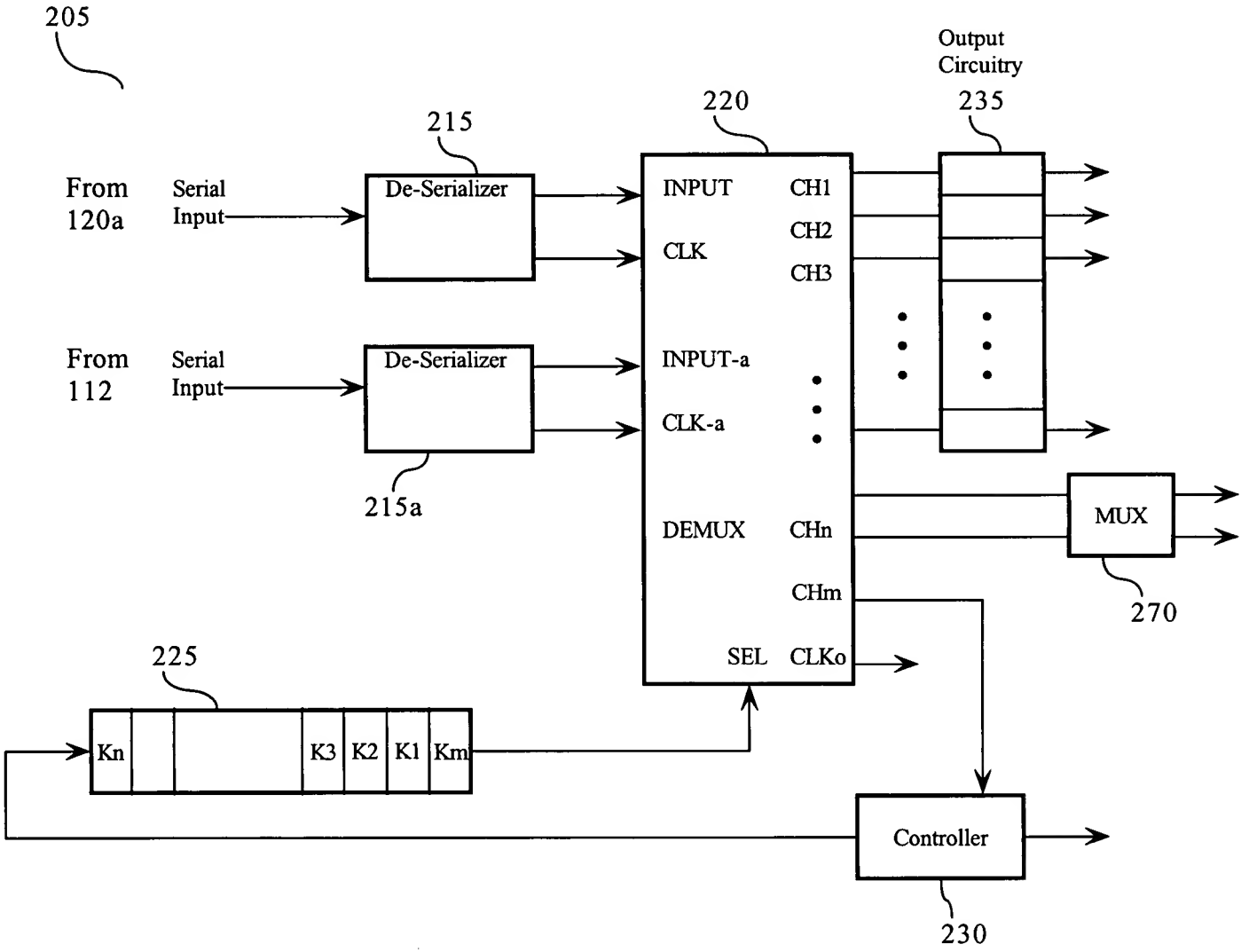
205
Output
Circuitry
235
220
215
From
120a
Serial
Input
De-Serializer
INPUT
CH1
CH2
CLK
CH3
From
112
Serial
Input
De-Serializer
INPUT-a
CLK-a
215a
MUX
DEMUX
CHn
CHm
270
SEL
CLKo
225
Kn
K3
K2
K1
Km
Controller
230

Fig. 3

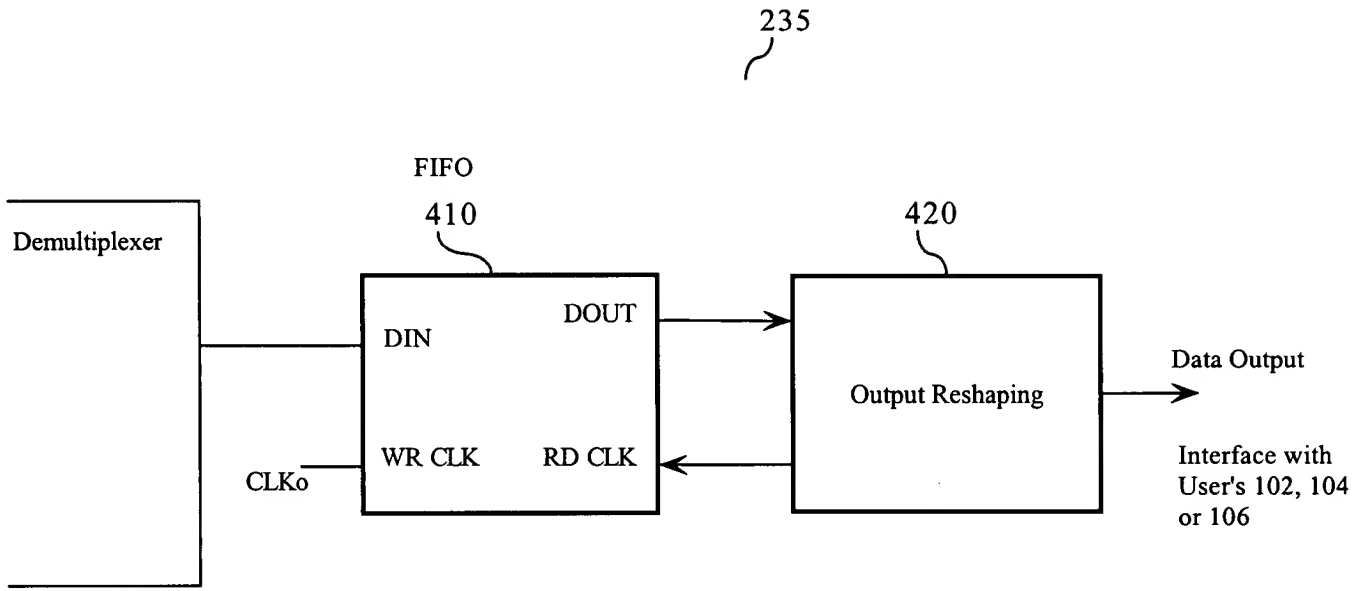
235
FIFO
410
420
Demultiplexer
DIN
DOUT
WR CLK
RD CLK
CLKo
Output Reshaping
Data Output
Interface with
User's 102, 104
or 106

Fig. 4

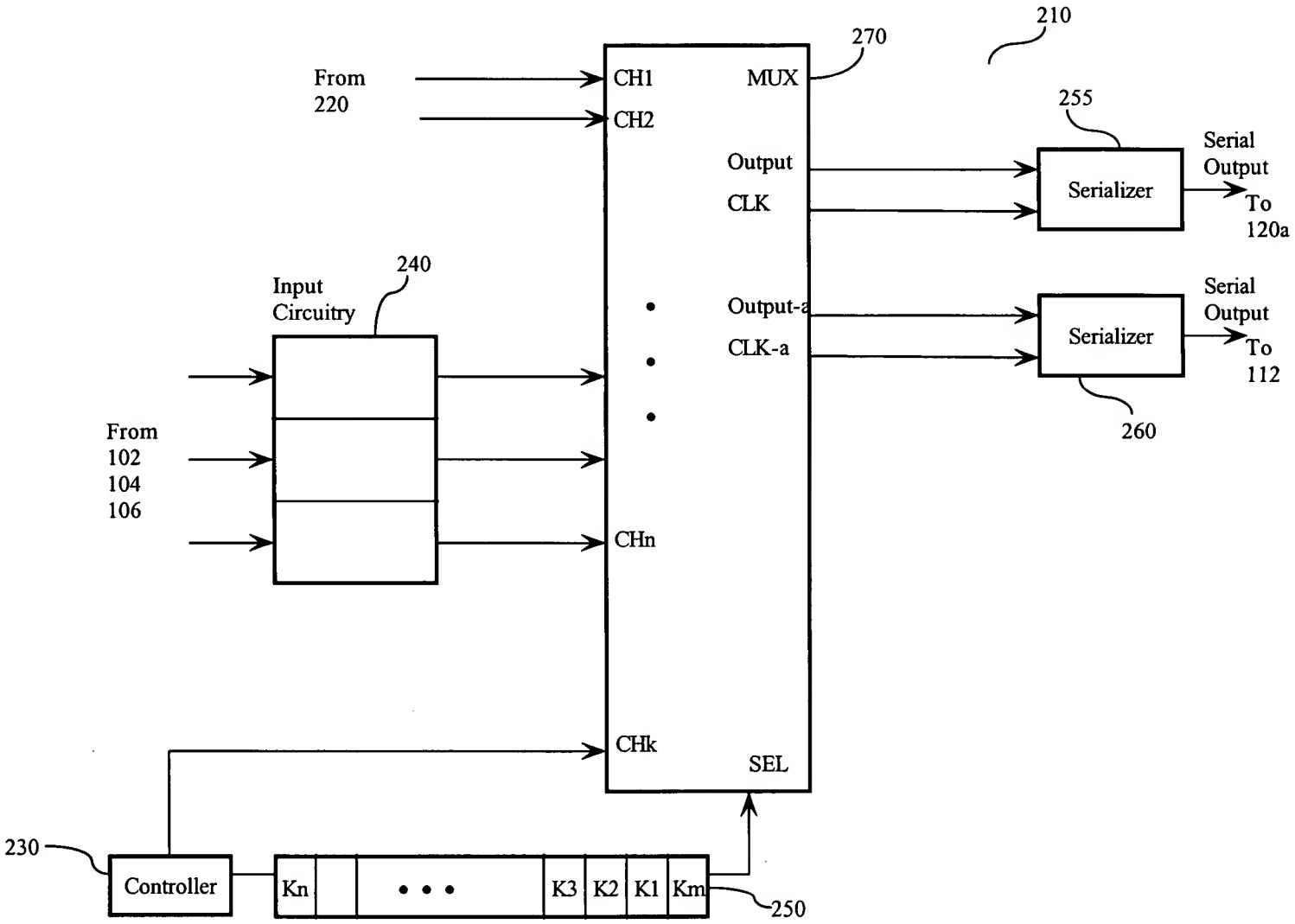
210
270
From
220
CH1
CH2
MUX
Output
CLK
255
Serializer
Serial
Output
To
120a
240
Input
Circuitry
Output-a
CLK-a
Serializer
Serial
Output
To
112
From
102
104
106
260
CHn
CHk
SEL
230
Controller
Kn
K3
K2
K1
Km
250

Fig. 5

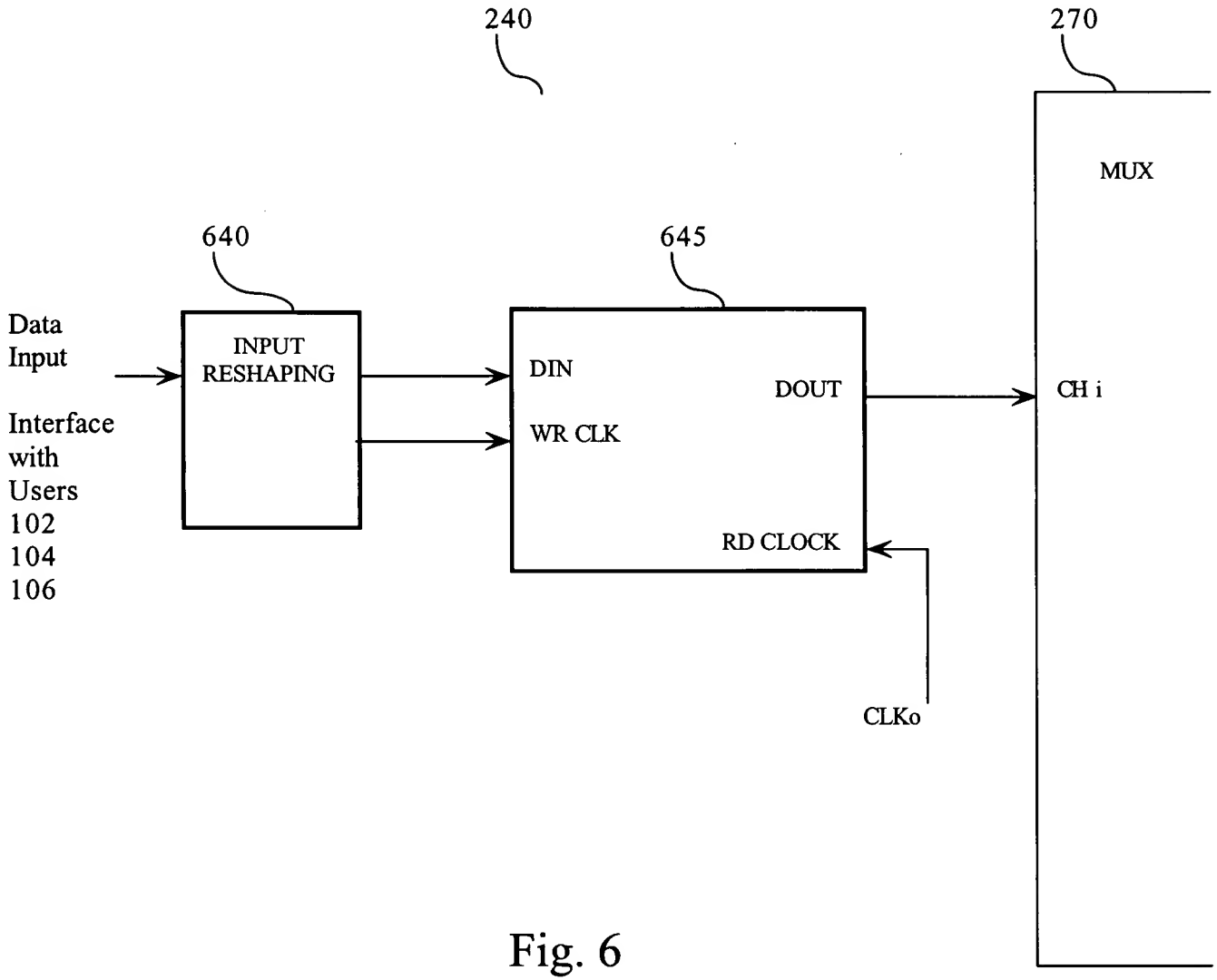
240
270
MUX
640
645
Data
Input
Interface
with
Users
102
104
106
INPUT
RESHAPING
DIN
WR CLK
DOUT
RD CLOCK
CH i
CLKo

Fig. 6

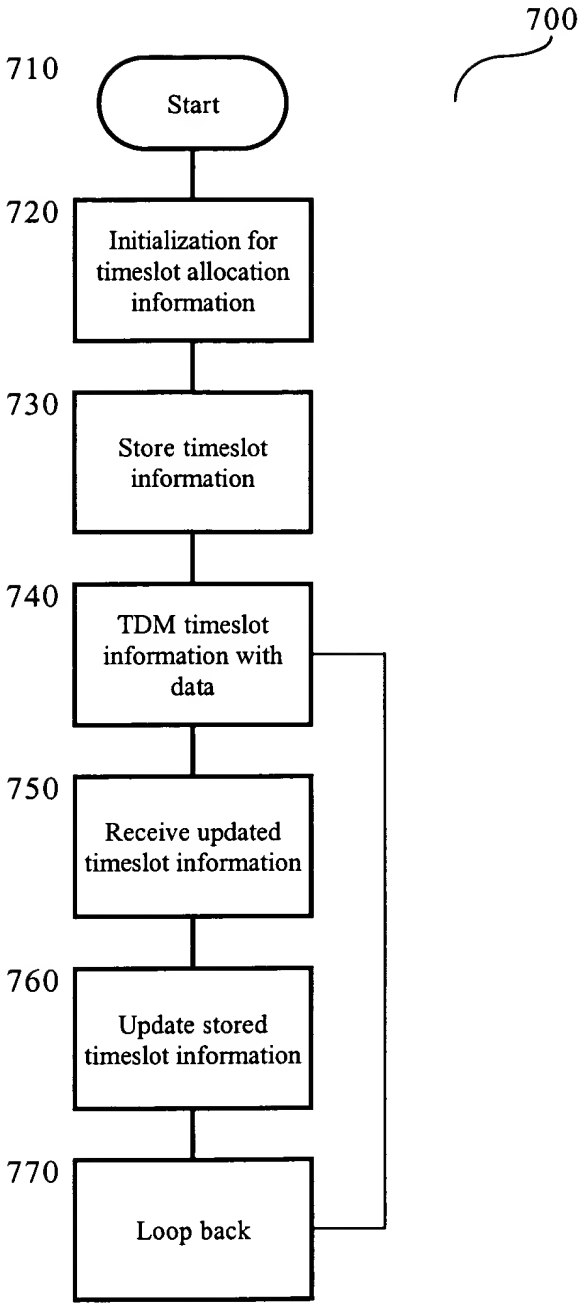
700
710
Start
720
Initialization for timeslot allocation information
730
Store timeslot information
740
TDM timeslot information with data
750
Receive updated timeslot information
760
Update stored timeslot information
770
Loop back

Fig. 7

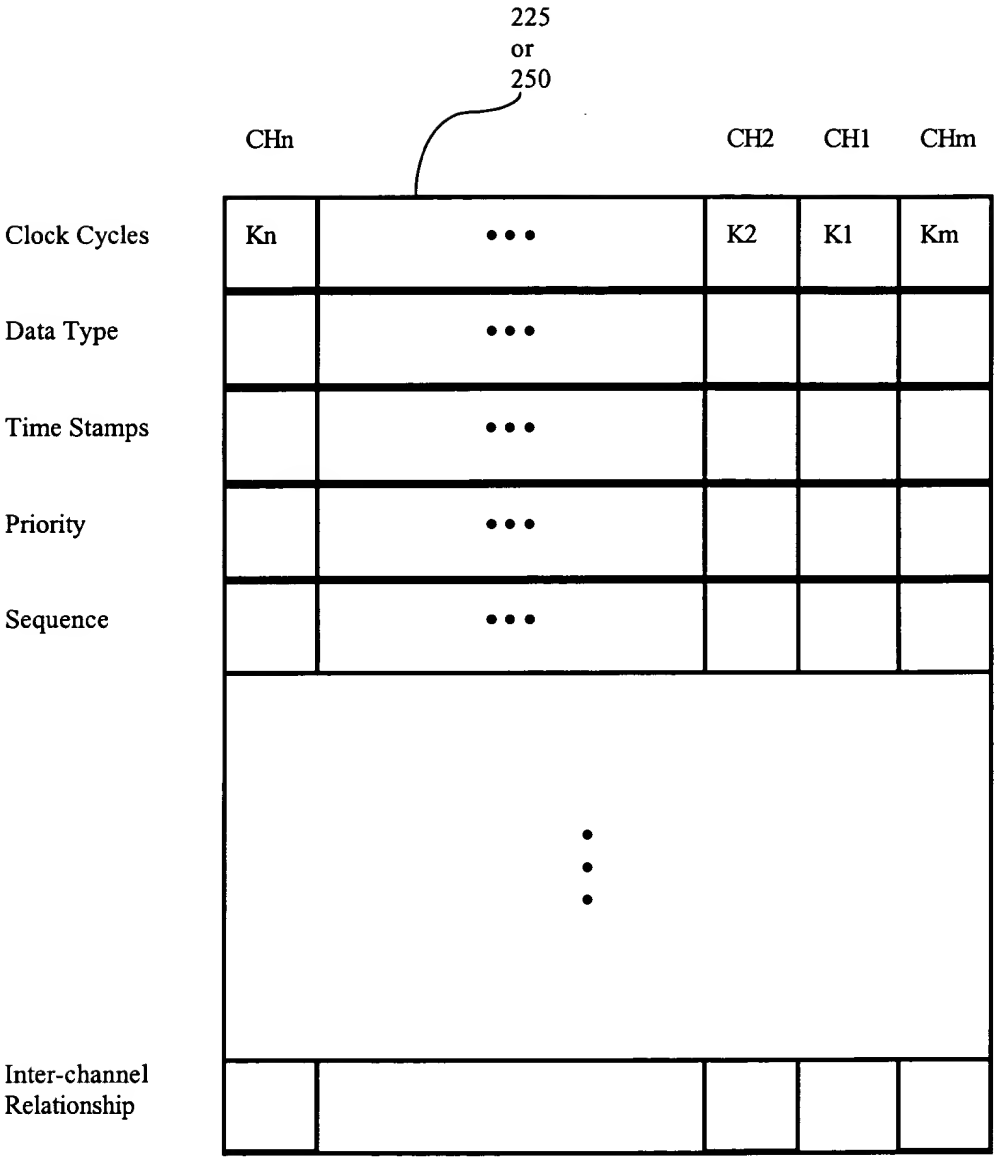
225
or
250
CHn
CH2
CH1
CHm
Clock Cycles
Kn
K2
K1
Km
Data Type
Time Stamps
Priority
Sequence
Inter-channel
Relationship

Fig.8